Interference Search

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("third bus is provided with a secondary cache")	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41
L2	91	(memory same cacheable near5 non-cacheable).clm.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41
L3	7	("semiconductor data processor"). clm.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41
L4	46	(memory same cacheable near5 non-cacheable).clm. and (read buffer).clm.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41
L5	3	first near memory near5 second near memory same cacheable near5 non-cacheable	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41
L6	0	"third bus is provided with a secondary cache".clm.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:41

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	191	third with bus with cache and memory adj controller	US-PGPUB; USPAT	OR	ON	2007/10/14 17:32
L2	25275	(upstream adj side) same (downstream adj side)	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L3	28	(read adj buffer) near memory with cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L4	17789	processor.ti.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L5	342	711/138.ccls.	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L6	23	L4 and L5	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L7	15	semiconductor near processor and "L2" near cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
L8	25	third adj bus with cache and memory adj controller	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
L9	31141	level adj "2"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
L10	21	semiconductor near data near processor	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
L11	6	L9 and L10	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
L12	1487	"non-cacheable"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:35
L13	882	"non-cacheable" and (main adj memory) not print	US-PGPUB; USPAT	OR	ON	2007/10/14 17:35
L14	5	(third adj bus) same "L2" same "L1"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
L15	4	(third adj bus) same between same "L2" same "L1"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
L16	1361	level adj "2" adj cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
L17	51	main adj memory near level near cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
L19	26	16 and 17	US-PGPUB; USPAT	OR	ON	2007/10/14 17:37
L21	1	1 and 3	US-PGPUB; USPAT	OR	ON	2007/10/14 17:37
S1	7	semiconductor adj data adj processor.clm.	US-PGPUB; USPAT	OR	ON	2006/11/15 11:52
S2	7	(semiconductor adj data adj processor).clm.	US-PGPUB; USPAT	OR	ON	2007/06/16 18:37

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S3	1	10/520,653	US-PGPUB; USPAT	OR	ON	2006/11/02 11:56
S4	0	10/32,615	US-PGPUB; USPAT	OR	ON	2006/11/02 12:01
S5	2	10/320,615	US-PGPUB; USPAT	OR	ON	2006/11/02 12:01
S6	7	(semiconductor adj data adj processor).clm.	US-PGPUB; USPAT	OR	ON	2006/11/07 13:38
S7	27	accessed and as and non near cacheable adj area	US-PGPUB; USPAT	OR	ON	2006/11/07 14:13
S9	220460	data and transfer and controller	US-PGPUB; USPAT	OR	ON	2006/11/08 14:02
S10	5956	data and transfer and controller.ti.	US-PGPUB; USPAT	OR	ON	2006/11/08 14:03
S11	131	(data and transfer and controller). ti.	US-PGPUB; USPAT	OR	ON	2006/11/08 14:05
S14	24	third adj bus with cache and memory adj controller	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
S16	15	(second adj memory and cacheable near non-cacheable). clm.	US-PGPUB; USPAT	OR	ON	2006/11/14 10:56
S17	16295	processor.ti.	US-PGPUB; USPAT	OR	ON	2006/11/14 10:59
S19	36	processor.ti. and second adj memory adj controller	US-PGPUB; USPAT	OR	ON	2006/11/14 11:00
S20	319	711/138.ccls.	US-PGPUB; USPAT	OR	ON	2006/11/14 11:00
S21	0	S19 and S20	US-PGPUB; USPAT	OR	ON	2006/11/14 11:00
S22	22	S17 and S20	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
S23	14	semiconductor near processor and "L2" near cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33
S24	91653	"L2"	US-PGPUB; USPAT	OR	ON	2006/11/15 10:20
S25	0	(2002/0173296).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/11/15 10:21
S26	1	("20020173296").PN.	US-PGPUB; USPAT	OR	OFF	2006/11/15 10:21
S27	27702	level adj "2"	US-PGPUB; USPAT	OR	ON	2006/11/15 11:48
S28	1164	level adj "2" adj cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36

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S29	75	(level adj "2" adj cache) and (second adj memory) and (main adj memory)	US-PGPUB; USPAT	OR	ON	2006/11/15 16:36
S32	48	main adj memory near level near cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
S33	18	semiconductor near data near processor	US-PGPUB; USPAT	OR	ON	2006/11/15 15:20
S34	0	S32 and S33	US-PGPUB; USPAT	OR	ON	2006/11/15 11:53
S35	6	S27 and S33	US-PGPUB; USPAT	OR	ON	2007/10/14 17:34
S36	1320	"non-cacheable"	US-PGPUB; USPAT	OR	ON	2006/11/15 12:03
S38	56	S36 and S28	US-PGPUB; USPAT	OR	ON	2006/11/15 12:04
S45	9	"5812418"	US-PGPUB; USPAT	OR	ON	2006/11/15 15:22
S54	1	"11060037"	US-PGPUB; USPAT	OR	ON	2006/11/15 17:31
S59	1	"6134641".pn.	US-PGPUB; USPAT	OR	ON	2006/12/11 08:52
S60	1330	"non-cacheable"	US-PGPUB; USPAT	OR	ON	2006/12/06 08:40
S61	908	"non-cacheable" and (main adj memory)	US-PGPUB; USPAT	OR	ON	2006/12/06 08:43
S62	809	"non-cacheable" and (main adj memory) not print	US-PGPUB; USPAT	OR	ON	2007/10/14 17:35
S63	320	711/138.ccls.	US-PGPUB; USPAT	OR	ON	2006/12/06 08:55
S64	51	S60 and S63	US-PGPUB; USPAT	OR	ON	2006/12/06 11:22
S65	2	"5,701,425"	US-PGPUB; USPAT	OR	ON	2006/12/06 11:28
S66	17	"5432943"	US-PGPUB; USPAT	OR	ON	2006/12/06 15:49
S67	37	"5410669"	US-PGPUB; USPAT	OR	ON	2006/12/08 13:13
S68	0	"08871295"	US-PGPUB; USPAT	OR	ON	2006/12/08 13:13
S69	0	"08871295".ap.	US-PGPUB; USPAT	OR	ON	2006/12/08 13:13
S70	0	"08/871295".ap.	US-PGPUB; USPAT	OR	ON	2006/12/08 13:13

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S71	1	08/871295	US-PGPUB; USPAT	OR	ON	2006/12/08 13:14
S72	20	dual adj purpose adj memory	US-PGPUB; USPAT	OR	ON	2006/12/08 13:53
S73	1	"6678790".pn.	US-PGPUB; USPAT	OR	ON	2006/12/08 13:54
S74	13	("5067078" | "5155833" | "5367653" | "5410669" | "5586293" | "5651134" | "5680363" | "5721862" | "5819305" | "5822755" | "5835941" | "5835956" | "5850632").PN. OR ("6678790"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/12/08 13:54
S75	2	"6678790"	US-PGPUB; USPAT	OR	ON	2006/12/08 14:10
S77	4098	data and processor and "L1" and "L2" and cache and bus	US-PGPUB; USPAT	OR	ON	2006/12/08 15:23
S78	32	(third adj bus) and data and processor and "L1" and "L2" and cache	US-PGPUB; USPAT	OR	ON	2006/12/08 15:24
S79	9	("5175864").URPN.	USPAT	OR	ON	2006/12/08 17:30
S80	2141	((first adj memory) and (second adj memory) and (read with write)).clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 08:53
S81	330	(processor same (first adj memory) and (second adj memory) and (read with write)). clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 08:54
S82	140	(processor same (first adj memory) and (second adj memory) same (read with write)). clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 09:00
S83	0	(processor same (first adj memory) near (second adj memory) near (read with write)). clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 09:01
S84	84	(processor same (first adj memory) same (second adj memory) same (read with write)). clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 09:59
S85	1	(processor same (first adj memory) same (second adj memory) same (read adj buffer)). clm.	US-PGPUB; USPAT	OR	ON	2006/12/11 09:01
S86	1	"11374048"	US-PGPUB; USPAT	OR	ON	2006/12/11 10:00

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S87	2	"10241458"	US-PGPUB; USPAT	OR	ON	2006/12/11 10:01
S88	0	"11276004"	US-PGPUB; USPAT	OR	ON	2006/12/11 10:01
S89	1	"20060095683"	US-PGPUB; USPAT	OR	ON	2006/12/11 10:05
S90	0	"10523517"	US-PGPUB; USPAT	OR	ON	2006/12/11 10:05
S91	1	"20050235111"	US-PGPUB; USPAT	OR	ON	2006/12/11 15:31
S92	312208	upstream	US-PGPUB; USPAT	OR	ON	2006/12/11 15:31
S93	43306	upstream adj side	US-PGPUB; USPAT	OR	ON	2006/12/11 15:31
S95	19124	(upstream adj side) with (downstream adj side)	US-PGPUB; USPAT	OR	ON	2006/12/11 15:33
S96	25	(upstream adj side) with (downstream adj side) same data same buffer	US-PGPUB; USPAT	OR	ON	2006/12/11 16:50
S98	2021	711/118.ccls.	US-PGPUB; USPAT	OR	ON	2006/12/11 16:50
S99	1	(third adj bus) same connecting same "L2" same "L1"	US-PGPUB; USPAT	OR	ON	2006/12/12 09:06
S100	3	(third adj bus) same between same "L2" same "L1"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:36
S101	4	(third adj bus) same "L2" same "L1"	US-PGPUB; USPAT	OR	ON	2007/10/14 17:35
S102	1	(third adj bus) near "L2" with "L1"	US-PGPUB; USPAT	OR	ON	2006/12/12 09:07
S103	2014	(third adj bus)	US-PGPUB; USPAT	OR	ON	2006/12/12 09:07
S104	1	(third adj bus) same "secondary memory"	US-PGPUB; USPAT	OR	ON	2006/12/12 09:08
S105	1	(third adj bus) same "secondary cache"	US-PGPUB; USPAT	OR	ON	2006/12/12 09:08
S106	94	(third adj bus) same cache	US-PGPUB; USPAT	OR	ON	2006/12/12 10:31
S107	0	"6678790".pn. and internal	US-PGPUB; USPAT	OR	ON	2006/12/12 10:31
S108	1	"6678790".pn. and memory	US-PGPUB; USPAT	OR	ON	2006/12/12 10:32
S109	10	"6606686"	US-PGPUB; USPAT	OR	ON	2007/06/15 19:23

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S110	6	"6606686" and buffer	US-PGPUB; USPAT	OR	ON	2007/06/15 19:25
S111	5	"6606686" and read adj cache	US-PGPUB; USPAT	OR	ON	2007/06/15 19:25
S112	0	(read adj buffer) same (dual adj purpose adj memory)	US-PGPUB; USPAT	OR	ON	2007/06/16 18:38
S113	8556	(read adj buffer) same5 (dual adj purpose adj memory)	US-PGPUB; USPAT	OR	ON	2007/06/16 18:38
S114	0	(read adj buffer) and (dual adj purpose adj memory)	US-PGPUB; USPAT	OR	ON	2007/06/16 18:38
S115	28	(read adj buffer) near memory with cache	US-PGPUB; USPAT	OR	ON	2007/10/14 17:33